CLAIMS:

1. A display apparatus for executing display by independently applying a signal to each pixel of a group of pixels arranged in matrix, by use of lead wires arranged in row and column directions, comprising display control means for displaying a compressed image signal without developing it to a bit map in which each pixel has gray scale information.

2. A display apparatus for executing display by independently applying a signal to each pixel of a group of pixels arranged in matrix, by use of lead wires arranged in row and column directions, comprising display control means for expanding a compressed image signal to gray scale information for each pixel, disposed inside each pixel.

3. A display apparatus for executing display by independently applying a signal to each pixel of a group of pixels arranged in matrix, by use of lead wires arranged in row and column directions, comprising display control means for displaying as such a compressed image signal without increasing a data quantity of said image signal.

4. A display apparatus according to claim 1, wherein said image signal is an image signal compressed by a spatial axis and a gray scale axis.

5. A display apparatus according to claim 1, wherein, when said pixels are arranged to in N rows x N' columns to constitute a block, a gray scale signal

having an n value smaller than N x N' is defined by a look-up table and is transferred to each of said blocks, and an identification signal for said gray scale signal is transferred to each of said pixels inside said block.

6. A display apparatus according to claim 1, wherein, when said pixels are arranged in N rows x N' columns to constitute a block, a gray signal having an n value smaller than N x N' is defined by a look-up table and is transferred to only said blocks having a great gray scale change among a plurality of frames, and an identification signal for said gray scale signal is transferred to each of said pixels inside said block.

7. A display apparatus according to claim 1, wherein, when said pixels are arranged in N rows x N' columns to constitute a block, a gray scale signal having an m value smaller than N x N' is defined by a look-up table covering a plurality of frames and is transferred, and an identification signal for said gray scale signal for a plurality of frames is transferred to each of said pixels inside said block, whereas in blocks having a large gray scale change among a plurality of frames, a gray scale signal having an n value smaller than N x N' and smaller than said m value is defined by a look-up table for a single frame and is transferred, and an identification signal inside a single frame for said gray scale signal is transferred

to each of said pixels inside said block.

8. A display apparatus according to claim 5, wherein said display control means gives an identification signal for n gray scale signals defined for a pixel block of N rows x N' columns to said pixel block, and then gives one of said gray scale signals of the n gray scales to each of said pixels on the basis of said identification signal.

9. A display apparatus according to claim 5, wherein said display control means gives said identification signal for said n gray scales to be given to a next pixel block of N rows x N' columns to each pixel of said next block during the same period in which said n gray scale signals defined for a pixel block of the N rows x N' columns are given to each of said pixels to which said identification signal is allocated.

10. A display apparatus according to claim 5, wherein said display control means gives said identification signal for one of said gray scale signals of said n gray scales to be given to a next pixel block of N rows x N' columns to corresponding one of said pixels of said next block during the same period in which said identification signal is given to said pixel to which said gray scale is allocated, as to one of said n gray scale signals defined for a pixel block of the N rows x N' columns.

11. A display apparatus comprising:

pixels arranged in matrix in a row direction and in a column direction;

a pixel electrode disposed inside each of said pixels;

a display device disposed inside each of said pixels, for executing display in accordance with a voltage of said pixel electrode;

a scanning line driving circuit for supplying a scanning signal to a scanning line;

an identification signal line driving circuit for supplying an identification signal to an identification signal line so disposed as to substantially cross said scanning line;

storage means for storing said identification signal supplied from said identification signal line in said pixel;

a gray scale voltage line driving circuit for supplying a gray scale voltage to at least two gray scale voltage lines for supplying said gray scale voltage to each of said pixels;

selection means for selecting said gray scale voltage supplied to said gray scale voltage lines on the basis of said identification signal stored in said storage means;

a switching device for applying said selected gray scale voltage to said pixel electrode; and

a gray scale write line driving circuit for supplying a gray scale write signal to a gray scale

write line for controlling said switching device.

12. A display apparatus according to claim 11, wherein said display device comprises a light modulator using a liquid crystal; two said gray scale voltage lines are provided to one pixel; said storage means comprises a first active device connected to said identification signal line by use of said scanning line as a gate terminal and a pixel internal memory capacitance; said selection means comprises n and p type active devices having a gate terminal thereof connected to said memory internal capacitance, and connected to said two gray scale voltage lines, respectively; and said switching device comprises an n type active device and a p type active device using said gray scale write line as a gate terminal, and a fourth active device connected to said pixel electrode.

13. A display apparatus according to claim 12, wherein, in a first stage of display, said first active device connected to a selected scanning line becomes conductive, an identification signal is written into said pixel internal memory capacitance of each of said pixels, and said identification signal renders either one of said n and p type active devices conductive to thereby decide the voltage of either one of said two gray scale signal lines; and in a second stage of display, said gray scale write line is selected to thereby render said fourth active device conductive, the voltage of said gray scale signal line so decided

is applied to said pixel electrode and changes the alignment of said liquid crystal, and light is modulated.

14. A display apparatus according to claim 11, wherein two said gray scale voltage lines are disposed for one pixel; said storage means comprises a first active device connected to said identification signal line by use of said scanning line as a gate terminal, and a pixel internal memory capacitance; said selection means comprises an n type active device and a p type active device having a gate terminal thereof connected to said pixel internal memory capacitance, and connected to said two gray scale voltage lines, respectively; said switching device comprises n and p type active devices using said gray scale write line as a gate terminal, and a fourth active device connected to said pixel electrode; and said display device is an LED device driven by a fifth active device using said pixel electrode as a gate terminal.

15. A display apparatus according to claim 12, wherein, in a first stage of display, said first active device connected to a selected scanning line becomes conductive, an identification signal is written into said pixel internal memory capacitance of each of said pixels, and said identification signal renders either one of said n and p type active devices conductive to thereby decide the voltage of either one of said two gray scale signal lines; and in a second stage of

display, said gray scale write line is selected to thereby render said fourth active device conductive, the voltage of said gray scale signal line so decided is applied to said pixel electrode, and said fifth active device converts the voltage to a current and drives an LED.

16. A display apparatus comprising:

pixels arranged in matrix in a row direction and in a column direction;

a pixel electrode disposed inside each of said pixels;

a display device disposed inside each of said pixels, for executing display in accordance with a voltage of said pixel electrode;

a scanning line driving circuit for supplying a scanning signal to a scanning line;

an identification signal line driving circuit for supplying an identification signal to an identification signal line so disposed as to substantially cross said scanning line;

storage means for storing said identification signal supplied from said identification signal line in said pixel;

a gray scale voltage line driving circuit for supplying a gray scale voltage to at least one gray scale voltage line for supplying said gray scale voltage to each of said pixels;

selection means for selecting said gray scale

voltage supplied to said gray scale voltage lines of said pixel adjacent to each other or to said gray scale voltage line of own pixel on the basis of said identification signal stored in said storage means;

a switching device for applying said selected gray scale voltage to said pixel electrode; and

a gray scale write line driving circuit for supplying a gray scale write signal to a gray scale write line for controlling said switching device.

17. A display apparatus according to claim 16, wherein said display device comprises a light modulator using a liquid crystal; two said gray scale voltage lines are provided to one pixel; said storage means comprises a first active device connected to said identification signal line by use of said scanning line as a gate terminal and a pixel internal memory capacitance; said selection means comprises n and p type active devices having a gate terminal thereof connected to said pixel internal memory capacitance, and connected to said pixels adjacent to each other and to said two gray scale voltage lines of own pixel, respectively; and said switching device comprises an n type active device and a p type active device using said gray scale write line as a gate terminal, and a fourth active device connected to said pixel electrode.

18. A display apparatus according to claim 17, wherein, in a first stage of display, said first active device connected to a selected scanning line becomes

conductive, an identification signal is written into said pixel internal memory capacitance of each of said pixels, and said identification signal renders either one of said n and p type active devices conductive to thereby decide the voltage of either one of said two gray scale signal lines inside said pixels adjacent to each other; and in a second stage of display, said gray scale write line is selected to thereby render said fourth active device conductive, the voltage of said gray scale signal line so decided is applied to said pixel electrode and changes the alignment of a liquid crystal, and light is modulated.

19. A display apparatus comprising:

pixels arranged in matrix in a row direction and in a column direction;

a pixel electrode disposed inside each of said pixels;

a display device disposed inside each of said pixels, for executing display in accordance with a voltage of said pixel electrode;

a scanning line driving circuit for supplying a scanning signal to a scanning line;

an identification signal line driving circuit for supplying an identification signal to an identification signal line so disposed as to substantially cross said scanning line;

storage means for storing said identification signal supplied from said identification signal line in

said pixel;

a gray scale voltage line driving circuit for supplying a gray scale voltage to at least two gray scale voltage lines for supplying said gray scale voltage to each of said pixels;

selection means for selecting said gray scale voltage supplied to said gray scale voltage lines on the basis of said identification signal stored in said storage means;

a switch for outputting said selected gray scale voltage to said pixel electrode;

an area control line driving circuit for supplying an area control signal to an area control line for controlling said switch;

a switching device for applying said gray scale voltage outputted from said switch to said pixel electrode; and

a gray scale write line driving circuit so disposed as to substantially cross said area control line, for supplying a gray scale write signal to a gray scale write line for controlling said switching device.

20. A display apparatus according to claim 19, wherein said display device comprises a light modulator using a liquid crystal; two said gray scale voltage lines are provided to one pixel; said storage means comprises a first active device connected to said identification signal line by use of said scanning line as a gate terminal and a pixel internal memory

capacitance; said selection means comprises n and p type active devices having a gate terminal thereof connected to said pixel internal memory capacitance, and connected to said two gray scale voltage lines, respectively; said switch is an active device using said area control line as a gate terminal and connected to said n and p type active devices; and said switching device comprises a fourth active device using said gray scale write line as a gate terminal and connected to said active device and to said pixel electrode.

21. A display apparatus according to claim 20, wherein, in a first stage of display, said first active device connected to a selected scanning line becomes conductive, an identification signal is written into said pixel internal memory capacitance of each of said pixels, and said identification signal renders either one of said n and p type active devices conductive to thereby decide the voltage of either one of said two gray scale signal lines; and in a second stage of display, said area control line and said gray scale write line are selected to thereby render said active device and said fourth active device conductive, the voltage of said gray scale signal line is applied to said pixel electrode and changes the alignment of a liquid crystal in said pixel designated by said area control line and said gray scale write line, and light is modulated.

22. A display apparatus comprising:

pixels arranged in matrix in a row direction and in a column direction;

a pixel electrode disposed inside each of said pixels;

a display device disposed inside each of said pixels, for executing display in accordance with a voltage of said pixel electrode;

a scanning line driving circuit for supplying a scanning signal to a scanning line;

an identification signal line driving circuit for supplying an identification signal to an identification signal line so disposed as to substantially cross said scanning line;

storage means for storing said identification signal supplied from said identification signal line in said pixel;

a gray scale voltage line driving circuit for supplying a gray scale voltage to at least one gray scale voltage line for supplying said gray scale voltage to each of said pixels;

selection means for selecting whether or not said gray scale voltage supplied to said gray scale voltage lines is to be outputted, on the basis of said identification signal stored in said storage means;

a switching device for applying said gray scale voltage selected and outputted from said selection means to said pixel electrode;

a gray scale write line driving circuit for

supplying a gray scale write signal to a gray scale write line for controlling said switching device; and

a line memory for temporarily storing data to said identification signal line driving circuit and to said gray scale voltage line driving circuit.

23. A display apparatus according to claim 22, wherein said display device comprises a light modulator using a liquid crystal; one said gray scale voltage line is provided to one pixel; said storage means comprises a first active device connected to said identification signal line by use of said scanning line as a gate terminal and a pixel internal memory capacitance; said selection means comprises a second active device having a gate terminal thereof connected to said pixel internal memory capacitance, and connected to said gray scale voltage line; and said switching device comprises a fourth active device using said gray scale write line as a gate terminal, and connected to said second active device and to said pixel electrode.

24. A display apparatus according to claim 23, wherein, in a first stage of display, said first active device connected to a selected scanning line becomes conductive, and an identification signal for the first gray scale is written into said pixel internal memory capacitance of each of said pixels and controls the conduction state of said second active device to thereby decide whether or not the gray scale voltage is

to be outputted; in a second stage of display, when said gray scale write line is selected, said fourth active device becomes conductive, the voltage of said gray scale signal line is applied to said pixel electrode in said pixel outputting the voltage for the first gray scale to thereby change the alignment of said liquid crystal, and light is modulated; in a third stage of display, said first active device connected to said scanning line once again selected becomes conductive, said identification signal for the second gray scale is written into said pixel internal memory capacitance of each of said pixels and controls the conduction state of said second active device to thereby decide whether or not said gray scale voltage is outputted; and in a fourth stage of display, when said gray scale write line is selected, said fourth active device becomes conductive, the voltage of said gray scale signal line is applied to said pixel outputting the voltage corresponding to the second gray scale to thereby change the alignment of said liquid crystal, and light is modulated; each of said display stages being repeated up to a 2n-th stage when n gray scales are defined for pixel blocks of N rows x N' columns.

25. A display apparatus comprising:

pixels arranged in matrix in a row direction and in a column direction;

a pixel electrode disposed inside each of

said pixels;

a display device disposed inside each of said pixels, for executing display in accordance with a voltage of said pixel electrode;

a scanning line driving circuit for supplying a scanning signal to a scanning line;

an identification signal line driving circuit for supplying an identification signal to an identification signal line so disposed as to substantially cross said scanning line;

storage means for storing said identification signal supplied from said identification signal line in said pixel;

a gray scale voltage line driving circuit for supplying a gray scale voltage to at least one gray scale voltage line for supplying said gray scale voltage to each of said pixels;

selection means for selecting whether or not said gray scale voltage supplied to said gray scale voltage lines is to be outputted on the basis of said identification signal stored in said storage means; and

a line memory for temporarily storing data to said identification signal line driving circuit and to said gray scale voltage line driving circuit.

26. A display apparatus according to claim 25, wherein said display device comprises a light modulator using a liquid crystal; one said gray scale voltage line is provided to one pixel; said storage means

comprises a first active device connected to said identification signal line by use of said scanning line as a gate terminal and a pixel internal memory capacitance; and said selection means comprises a second active device having a gate terminal thereof connected to said pixel internal memory capacitance and connected to said gray scale voltage line.

27. A display apparatus according to claim 26, wherein, in a first stage of display, said first active device connected to a selected scanning line becomes conductive, and an identification signal for the first gray scale is written into said pixel internal memory capacitance of each of said pixels; in a second stage of display, said identification signal controls the conduction state of said second active device and the first gray scale voltage is outputted to said pixel electrode; in a third stage, said scanning line is again selected, said first active device connected to said scanning line again selected becomes conductive, and said pixel internal memory capacitance of each of said pixels is reset by a rest signal applied to said identification signal line; in a fourth stage of display, said first active device connected to said scanning line again selected becomes conductive and said identification signal for the second gray scale is written into said pixel internal memory capacitance of each of said pixels; in a fifth stage of display, said identification signal controls the conduction state of

said second active device and the second gray scale voltage is outputted to said pixel electrode; and in a sixth stage of display, said scanning line is again selected, said first active device becomes conductive and the reset signal applied to said identification signal line resets said pixel internal memory capacitance of each of said pixels; each of said display stages being repeated up to a 3n-th stage when n gray scales are defined for pixel blocks of N rows x N' columns.

28. A display apparatus according to claim 23, wherein, when said pixel blocks consist of said pixels arranged in N rows x N' columns, the following process steps are conducted in blocks having a small gray scale change among a plurality of frames:

in a first stage of a first frame, said first active device connected to a selected scanning line becomes conductive, and an identification signal for the first gray scale is written into said pixel internal memory capacitance of each of said pixels and controls the conduction state of said second active device to thereby decide whether or not a gray scale voltage is to be outputted;

in a second stage, said fourth active device becomes conductive when said gray scale write line is selected, the voltage of said gray scale signal line is applied to said pixel electrode in said pixel outputting the voltage for the first gray scale to

thereby change the alignment of said liquid crystal, and light is modulated;

in a third stage, said first active device connected to said scanning line again selected becomes conductive, and an identification signal for the second gray scale is applied to said pixel internal memory capacitance of each of said pixels and controls the conduction state of said second active device to thereby decide whether or not the gray scale voltage is to be outputted;

in a fourth stage, said fourth active device becomes conductive when said gray scale write is selected, the voltage of said gray scale signal line is applied to said pixel electrode in said pixel outputting the voltage of the second gray scale to thereby change the alignment of said liquid crystal, and light is modulated;

in a first stage of a second frame, said first active device connected to a selected scanning line becomes conductive and said identification signal for the third gray scale is written into said pixel internal memory capacitance of each of said pixels and controls the conduction state of said second active device to thereby decide whether or not the gray scale voltage is to be outputted;

in a second stage, said fourth active device becomes conductive when said gray scale write line is selected, and the voltage of said gray scale signal

line is applied to said pixel electrodes in said pixel outputting the voltage for the third gray scale to thereby change the alignment of said liquid crystal, and light is modulated;

in a third stage, said first active device connected to said scanning line again selected becomes conductive, and an identification signal for a fourth gray scale is written into said pixel internal memory capacitance of each of said pixels and controls the conduction state of said second active device to thereby decide whether or not the gray scale voltage is to be outputted;

in a fourth stage, said fourth active device becomes conductive when said gray scale write line is selected, the voltage of said gray scale signal line is applied to said pixel electrode in said pixel outputting the voltage for the fourth gray scale and changes the alignment of said liquid crystal, and light is modulated; and

when m gray scales are defined for pixel blocks of N rows x N' columns having a small gray scale change among a plurality of frames and said stages in one frame are m' stages, said process steps are repeated up to an m/(m'/2)-th frame;

whereas in pixel blocks having a large gray scale change among a plurality of frames, the following process steps are executed;

in a first stage of each of said frames, said

first active device connected to a selected scanning line becomes conductive, said identification signal for the first gray scale is written into said pixel internal memory capacity of each of said pixels, and controls the conduction state of said second active device to thereby decide whether or not the gray scale voltage is to be outputted;

in a second stage, said fourth active device becomes conductive when said gray scale write line is selected, the voltage of said gray scale signal line is applied to said pixel electrode in said pixel outputting the voltage for the first gray scale to thereby change the alignment of said liquid crystal, and light is modulated;

in a third stage, said first active device connected to said scanning line again selected becomes conductive, said identification signal for the second gray scale is written into said pixel internal memory capacity of each of said pixels and controls the conduction state of said second active device to thereby decide whether or not the gray scale voltage is to be outputted; and

in a fourth stage, said fourth active device becomes conductive when said gray scale write line is selected, and the voltage of said gray scale signal line is applied to said pixel electrode in said pixel outputting the voltage for the second gray scale to thereby change the alignment of said liquid crystal,

and light is modulated; and

when n gray scales are defined for pixel blocks of N rows x N' columns having a large gray scale change among a plurality of frames, said stages inside one frame are repeated up to a 2n-th stage, and each of said frames is repeated each time.

29. A display apparatus according to claim 26, wherein, when said pixels are constituted into pixel blocks consisting of N rows x N' columns, the following process steps are conducted in blocks having a small gray scale change among a plurality of frames:

in a first stage of a first frame, said first active device connected to a selected scanning line becomes conductive, and an identification signal for the first gray scale is written into said pixel internal memory capacitance of each of said pixels;

in a second stage, said identification signal controls the conduction state of said second active device, the first gray scale voltage is outputted to said pixel electrode to thereby change the alignment of said liquid crystal, and light is modulated;

in a third stage, said scanning line is again selected, said first active device becomes conductive, and a reset signal applied to said identification signal line resets said pixel internal memory capacitance of each of said pixels;

in a fourth stage, said first active device connected to said scanning line again selected becomes

conductive, and an identification signal for the second gray scale is applied to said pixel internal memory capacitance of each of said pixels;

in a fifth state, said identification signal controls the conductions state of said second active device, the second gray scale voltage is applied to said pixel electrode to thereby change the alignment of said liquid crystal and light is modulated; and

in a sixth stage, said scanning line is again selected, said first active device becomes conductive and a reset signal applied to said identification signal line resets each of said pixel internal memory capacitance; and

in a first stage of the second frame, said first active device connected to said scanning line selected becomes conductive, and an identification signal for the third gray scale is written into said pixel internal memory capacitance of each of said pixels;

in a second stage, said identification signal controls the conduction state of said second active device, the third gray scale voltage is outputted to said pixel electrode to thereby change the alignment of said liquid crystal, and light is modulated;

in a third stage, said scanning line is again selected, said first active device becomes conductive and a reset signal applied to said identification signal line resets each of said pixel internal memory

capacitance;

in a fourth stage, said first active device connected to said scanning line again selected becomes conductive, and an identification signal for the fourth gray scale is written into each of said pixel internal memory capacitances;

in a fifth stage, said identification signal controls the conduction state of said second active device, the fourth gray scale voltage is outputted to said pixel electrode to thereby change the alignment of said liquid crystal and light is modulated; and

in a sixth stage, said scanning line is selected further again, said first active device becomes conductive and a reset signal applied to said identification signal line resets each of said pixel internal memory capacitances; and

when m gray scales are defined for pixel blocks of N rows x N' columns having a small gray scale change among a plurality of frames and said stages in one frame are m' stages, said process steps are repeated up to an m/(m'/3)-th frame;

whereas in a pixel block having a large gray scale change among a plurality of frames, the following process steps are executed;

in a first stage of each of said frames, said first active device connected to said scanning line selected becomes conductive, said identification signal for the first gray scale is written into said pixel

internal memory capacitance of each of said pixels;

in a second stage, said identification signal controls the conduction state of said second active device, the first gray scale is outputted to said pixel electrode to thereby change the alignment of said liquid crystal, and light is modulated;

in a third stage, said scanning line is again selected, said first active device becomes conductive, a reset signal applied to said identification signal line resets each of said pixel internal memory capacitances;

in a fourth stage, said first active device connected to said scanning line again selected becomes conductive and an identification signal for the second gray scale is written into said pixel internal memory capacitance inside each of said pixels;

in a fifth stage, said identification signal controls the conduction state of said second active device, the second gray scale voltage is outputted to said pixel electrode to thereby change the alignment of said liquid crystal and light is modulated; and

in a sixth stage, said scanning line is selected further again, said first active device becomes conductive and a reset signal applied to said identification signal line resets each of said pixel internal memory capacitances; and

when n gray scales are defined for pixel blocks of N rows x N' columns having a large gray scale

change among a plurality of frames, said stages inside one frame are repeated up to a 3n-th stage, and each of said frames is repeated each time.